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| 10/756,853 | 01/14/2004 | Norman Rubin | 00100.03.0023 | 3409 |

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| EXAMINER | |
|---|---|
| LAI, VINCENT | |
| **ART UNIT** | **PAPER NUMBER** |
| 2181 | |

DATE MAILED: 10/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/756,853 | RUBIN ET AL. | |
| | Examiner | Art Unit | |
| | Vincent Lai | 2181 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
10/6/2006

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Information Disclosure Statement*

1. The information disclosure statement (IDS) submitted on May 21, 2004 was considered by the examiner.

### *Response to Amendment*

2. Acknowledgment is made of the amendments to the specification, title, drawings and claims.

3. Objections to the title and claims are withdrawn after considering amendments.

4. The 35 USC 101 rejections are withdrawn after considering amendments.

### *Response to Arguments*

5. Applicant's arguments filed 2 August 2006 have been fully considered but they are not persuasive.

Applicant argues, "*Witt fails to teach or suggest, among other things, reading a context bit based on the plurality of extra bits.*" More specifically, Applicant argues the following:

*"Noticeably absent from the Office Action's characterization of Witt's disclosure is Applicant's claimed feature of a context bit separate from the plurality of extra bits."*

Examiner does not believe such a limitation is recited in the claims. Examiner was unable to find evidence of such limitations in claim 1 or any other claims.

*"The present Office Action appears to conflate the claimed setting of a context bit with the claimed plurality of extra bits associated with the first instruction."*

As explained above, it is the opinion of the Examiner that the claim language lends itself to the interpretation that it is possible for the two parts to be combined. Separation of the two is not apparent in the claims.

Applicant argues, "*The Office Action fails to identify "reading the context bit based on the plurality of extra bits.*"

Witt teaches that the context bit indicates whether an instruction is a branch or not (See column 6, lines 29-31). The extra bits (i.e. the don't care bits) are then indicative of branch information (See column 6, lines 31-34). In the case the context does not indicate a branch, then the don't care bits are ignored but they are used if the context does indicate a branch. Thus, the extra bits are necessary in conjunction to the context bit in certain contexts.

Applicant argues, "The 'state' or 'condition' of the control transfer bit does not appear in any way to effect whether the instruction is executed."

The claims do not reflect the idea that the 'state' or 'condition' does indeed effect whether the instruction is executed. Claim 1 merely states "executing the instruction when the context bit is in the first state." Witt does disclose execution of the instruction when it is in a first state.

### *Claim Objections*

6. Claim 8 is objected to because of the following informalities: It appears that the added limitation "memory device capable of storing a context bit" should be on its own line (i.e. a semicolon should follow "a processor having a context bit") and should instead read "memory devices capable of storing a context bit" since two devices are claimed later in the claim. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-2, 6, 8-9, 11-14, 16-17, and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Witt (U.S. Patent # 6,061,786), herein referred to as Witt.

As per **claim 1**, Witt discloses a method for nested control flow (See column 2, lines 7-9: A control flow change is called a control transfer), the method comprising:

setting a context bit (Control transfer bit: see column 6, lines 27-30) to at least one of: a first state and a second state (See column 6, lines 29-31: The two states are branch or not branch) receiving a first instruction having a plurality of extra bits (See column 6, lines 14-15: There are two bits of predecode information);

reading the context bit based on the plurality of extra bits (See column 6, lines 31-34: Such as in the case of don't cares); and

executing the instruction when the context bit is in the first state (See column 6, lines 29-31: Depending on the bit, the instruction is executed in one state or the other).

As per **claim 2**, Witt discloses further comprising: maintaining a counter value (See column 15, lines 59-62: The bimodal counter) wherein the counter value indicates a nesting depth of context bits that are set to a second state (See column 15, lines 62-65: The counter is incremented when a branch is taken).

As per **claim 6**, Witt discloses further comprising:

receiving a second instruction having a plurality of extra bits (See column 6, lines 14-15: There are two bits of predecode information);

reading the context bit based on the plurality of extra bits (See column 6, lines 31-34: Such as in the case of don't cares);

executing the second instruction when the context bit is in the first state (See column 6, lines 29-31: Depending on the bit, the instruction is executed in one state or the other); and

maintaining the counter value (See column 15, lines 62-65: The counter is incremented when a branch is taken).

As per **claim 8**, Witt discloses an apparatus for nested control flow (See column 2, lines 7-9: A control flow change is called a control transfer), the apparatus comprising:

a processor (Processor 10, see figure 1) having a context bit (Control transfer bit: see column 6, lines 27-30);

memory device[s] capable of storing a context bit (See figure 1, column 5, lines 30-42 and column 15, lines 59-65);

a first memory device storing a plurality of instructions (See figure 1, and column 5, lines 30-42: An instruction cache is present), wherein each of the plurality of instructions includes a plurality of extra bits (See column 6, lines 14-15: There are two bits of predecode information), and wherein the processor is operative to execute the plurality of instructions (All processors can execute instructions); and

a second memory device operably coupled to the processor, and wherein the second memory device receives an incrementing counter instruction upon the execution of one of the plurality of instructions (See column 15, lines 59-65: A counter is used with increments when a branch is taken).

As per **claim 9**, Witt discloses further comprising: a context bit memory device capable of storing the context bit (See figure 5: The context bits are saved in a register).

As per **claim 11**, Witt discloses wherein the processor receives a first instruction having a plurality of extra bits (See column 6, lines 14-15: There are two bits of predecode information) from the first memory device; and reads the context bit based on the plurality of extra bits (See column 6, lines 31-34: Such as in the case of don't cares).

As per **claim 12**, Witt discloses wherein the processor executes the first instruction when the context bit is read (See column 6, lines 29-31: Depending on the bit, the instruction is executed in one state or the other) and is in a first state; and maintains a counter value (See column 15, lines 59-62: The bimodal counter) wherein the counter value indicates a nesting depth of context bits that are set to a second state, using the incrementing counter instruction (See column 15, lines 62-65: The counter is incremented when a branch is taken).

As per **claim 13**, Witt discloses wherein the processor:

receives a second instruction having a plurality of extra bits (See column 6, lines 14-15: There are two bits of predecode information) from the first memory device;

reads the context bit based on the plurality of extra bits (See column 6, lines 31-34: Such as in the case of don't cares);

executes the second instruction when the context bit is in a first state; and

increments the counter bit value using the incrementing counter instruction (See column 6, lines 29-31: Depending on the bit, the instruction is executed in one state or the other).

As per **claim 14**, Witt discloses a graphics processing device comprising:

a plurality of arithmetic logic units (See column 11, lines 22-25: The functional units are responsible for execution of instructions and thus have at least one ALU), each of the plurality of arithmetic logic units having a context bit memory device capable of storing a context bit (Control transfer bit: see column 6, lines 27-30);

a first memory device storing a plurality of instructions (See figure 1, and column 5, lines 30-42: An instruction cache is present), wherein each of the plurality of instructions includes a plurality of extra bits (See column 6, lines 14-15: There are two bits of predecode information), and wherein the arithmetic logic units are operative to execute the plurality of instructions (All ALUs execute instructions); and

a second memory device operably coupled to the processor, wherein the second memory device receives an incrementing counter instruction upon the execution of one of the plurality of instructions (See column 15, lines 59-65: A counter is used with increments when a branch is taken).

As per **claim 16**, Witt discloses wherein each of the plurality of arithmetic logic units:

receive at least one of the plurality of instructions (See column 11, lines 22-25: ALUS receive instructions in order to be of use); and

reads the context bit based on the plurality of extra bits (See column 6, lines 31-34: Such as in the case of don't cares).

As per **claim 17**, Witt discloses wherein the plurality of arithmetic logic units execute the instructions when the context bit is read (See column 6, lines 29-31: Depending on the bit, the instruction is executed in one state or the other) and is in a first state; and

maintains a counter value (See column 15, lines 59-62: The bimodal counter) wherein the counter value indicates a nesting depth of context bits that are set to a second state, using the incrementing counter instruction (See column 15, lines 62-65: The counter is incremented when a branch is taken).

As per **claim 19**, Witt discloses a method for nested control flow, the method comprising:

setting a context bit (Control transfer bit: see column 6, lines 27-30) to at least one of: a first state and a second state (See column 6, lines 29-31: The two states are branch or not branch) receiving a first instruction having a plurality of extra bits (See column 6, lines 14-15: There are two bits of predecode information);

reading the context bit based on the plurality of extra bits (See column 6, lines 31-34: Such as in the case of don't cares);

executing the first instruction when the context bit is in the first state (See column 6, lines 29-31: Depending on the bit, the instruction is executed in one state or the other); and

upon the executing of the first instruction (See column 15, lines 59-62: The bimodal counter), wherein the counter value indicates a nesting depth of context bits that are set to a second state (See column 15, lines 62-65: The counter is incremented when a branch is taken) in a general purpose register.

As per **claim 20**, Witt discloses further comprising:

receiving a second instruction having a plurality of extra bits (See column 6, lines 14-15: There are two bits of predecode information);

reading the context bit based on the plurality of extra bits (See column 6, lines 31-34: Such as in the case of don't cares);

executing the second instruction when the context bit is in the first state (See column 6, lines 29-31: Depending on the bit, the instruction is executed in one state or the other); and

incrementing the counter value (See column 15, lines 62-65: The counter is incremented when a branch is taken).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3-4, 10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witt (U.S. Patent # 6,061,786), herein referred to as Witt.

As per **claims 3-4, 10 and 15**, Witt teaches the use of a counter value (See column 15, lines 59-62).

Witt does not teach storing a counter or the means to store a counter.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to store a counter in a non-dedicated memory device, wherein the non-dedicated memory device is a general purpose register. Storing a counter in a register is one of the simplest methods used and has been readily done in the field.

9. Claims 5, 7, 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witt (U.S. Patent # 6,061,786), herein referred to as Witt in view of Poland et al (U.S. Patent # 5,673,407), herein referred to as Poland et al.

As per **claim 5**, Witt teaches the use of context bits (Control transfer bit: see column 6, lines 27-30).

Witt does not teach resetting the counter value.

Poland et al teaches prior to setting the context bit, resetting the counter value (See column 14, lines 36-39: Values are reloaded after being zeroed at the end of an operation thus meaning a new context is necessary).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to reset the counter value since an incorrect counter would be of no use to determining a count and would be counterproductive.

As per **claim 7, 18, and 21**, Witt teaches the use of a counter value (See column 15, lines 59-62),

Witt does not teach exiting a nested control flow using the counter value.

Poland et al teaches terminating a computation processing using the counter (See column 14, lines 33-44: The counter is used as a timer as well and such a termination can be done with a time-out timer/counter).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to allow termination of processes using a counter because unchecked processes can tie up valuable resources/computation time, which would thus take away from any benefits the invention is meant to make.

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to show further art related to

method and apparatus for nested control flow utilizing extra bits as context information and a counter indicating nesting depth:

U.S. Patent # 5,692,168 to McMahan shows a prefetch buffer using flow control bit to identify changes of flow within the code stream.

U.S. Patent # 6,321,302 B1 to Strongin et al shows a stream read buffer for efficient interface with block oriented devices.

U.S. Patent # 6,717,576 B1 to Duluk, Jr. et al shows deferred shading graphics pipeline processing having advanced features.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

vl
March 31, 2006

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10/16/2006